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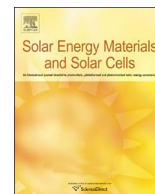
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Incorporation of CdSe layers into CdTe thin film solar cells

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ABSTRACT

Incorporation of CdSe layers into CdTe thin film solar cells has recently emerged as a route to improve cell performance. It has been suggested that the formation of lower band gap CdTe_(1-x)Se_x phases following Se diffusion induces bandgap grading which may increase the carrier lifetime and thereby open circuit voltage. In this study we investigate the impact of CdSe incorporation on CdTe solar cell performance. We demonstrate that the standard CdS/CdTe device architecture is incompatible with Se incorporation, owing to large optical losses. An alternative cell structure with an oxide partner layer replacing the CdS with SnO₂/CdSe/CdTe is developed, leading to cell efficiencies of > 13.5%. The differences in processing required for effective selenium incorporation are investigated with performance improvements resulting from additional post-growth annealing. Finally, other oxides such as TiO₂, ZnO and FTO are demonstrated to be unsuitable partner layers but highlight that the choice of partner layer is key to further improving the performance.

1. Introduction

CdTe has established itself as the most competitive of the thin-film photovoltaics (PV) technologies currently on the market, demonstrating high performance (> 22%), long-term stability and one of the lowest costs per kWh (~0.0387 \$ kWh) [1,2].

CdS was for a long time considered to be essential in achieving high performance. Cells produced without CdS (i.e. with a direct CdTe junction to the transparent conducting oxide electrode) have very low open circuit voltages (V_{OC}) and fill factors (FF), indicating that the CdTe/oxide interfaces were of inferior quality [3,4]. The primary benefit of CdS being that intermixing allows the formation of CdS_{1-x}Te_x and CdTe_{1-y}S_y phases which ease the lattice mismatch at the interface [5]. CdS is ultimately a limit to performance on account of its strong parasitic absorption in the 300–525 nm range (absorption in the CdS does not contribute to the photocurrent) [6,7]. Recent work has focused on the use of a CdSe layer to partner CdTe, either in addition to or as a replacement for CdS [2,8].

The use of a 1.7 eV band gap CdSe layer seems somewhat counter-intuitive as one would anticipate the increased optical absorption in this layer would act to reduce short circuit density (J_{SC}) compared to CdS, if the absorptions were similarly parasitic. It has been demonstrated though that during cell processing the CdSe diffuses into the CdTe, converting it from a photoinactive CdSe (wurtzite) phase to a

photoactive CdTe_(1-x)Se_x (zincblende) structure [4,8]. This has the effect of removing the unwanted CdSe layer, and replacing it with a lower band gap CdTe_(1-x)Se_x (≈ 1.36 eV) layer which increases photocurrent compared to CdTe. This means that in addition to a reduction in short wavelength losses [2,9], photon collection is extended to longer wavelengths. It has also been suggested that there is a bandgap grading within the CdTe_(1-x)Se_x layer resulting in a subsequent increase in carrier lifetime [9]. This change in the nature of the device junction via the incorporation of CdSe may make it possible to partner CdTe_(1-x)Se_x directly with simple oxide layers without the need for CdS. Cells produced using a CdTe_(1-x)Se_x structure without a CdS layer have so far shown reasonable performance, up to 14%, with the expected high current, but lower V_{OC} and FF values [4]. Thus far however little optimisation has been carried out on what is essentially a new interface structure.

In this work we report on the development of routes to effectively incorporate CdSe layers into CdTe solar cells. The device performance of cells produced with CdSe will be compared to those with CdS and CdS/CdSe. It will be shown that use of a CdS/CdSe layer structure has severe performance limitations and that device processing conditions need to be adjusted to effectively incorporate selenium. We also demonstrate that a TCO/CdSe structure is insufficient to maintain high performance and that an interlayer, such as SnO₂, is required between the TCO and CdSe layers, similar to the 'buffer' or 'high resistive

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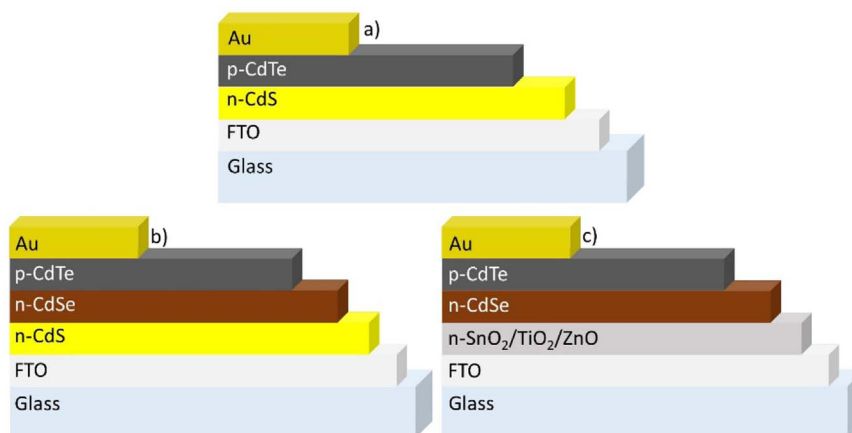


Fig. 1. A schematic representation of the device structures compared in this work, a) FTO/CdS/CdTe/Au, b) FTO/CdS/CdSe/CdTe/Au, c) FTO/(ZnO/TiO₂/SnO₂)/CdSe/CdTe/Au.

transparent' (HRT) layer structure often used in conjunction with CdS layers [10]. Other binary oxide partner layers, ZnO and TiO₂, are assessed for comparison to SnO₂. We demonstrate that use of a SnO₂ in a direct junction with CdTe_{(1-x)Se_x} and optimisation of the intermixing, allows the performance of CdS/CdTe devices to be matched. However, although this increases the J_{SC} , concomitant V_{OC} losses remain problematic.

2. Experimental

CdTe devices were produced in the conventional 'superstrate' configuration with a number of different layer structures being utilised for the readers reference devices compared in this work are shown in Fig. 1. All cells were deposited on NSG Ltd soda lime TEC™ 15 glass (F doped SnO₂ (FTO) coated glass). Unless otherwise stated 100 nm CdS was deposited via radio frequency (RF) sputtering at room temperature, using a chamber pressure of 5 mTorr (0.66 Pa) using Ar as the working gas and a power density of 1.32 W cm⁻². The base pressure reached in the sputtering chamber is 1.9×10^{-5} Torr (2.53 mPa). Varying thicknesses of layers were also deposited by RF sputtering at room temperature using a chamber pressure of 5 mTorr using Ar as the working gas and power density of 1.32 W cm⁻².

Layers between the TCO and CdSe layer were deposited by a variety of methods: undoped SnO₂ layers (100 nm) were deposited by chemical vapour deposition (CVD) at 600 °C. 100 nm of ZnO was deposited via RF sputtering at room temperature, using a chamber pressure of 5 mTorr using Ar as the working gas and a power density of 2.19 W cm⁻². 50 nm TiO₂ was deposited in a two-step process via spin-coating at 3000 rpm⁻¹ for 30 s from titanium isopropoxide in ethanol. The first stage was the deposition of a 0.15 M solution which was then pre-annealed at 110 °C for 10 min, followed by a second deposition of a 0.3 M solution which was again annealed at 110 °C for 10 min. The bilayer was then heated at 550 °C for 30 min in air.

Close space sublimation (CSS) was used to deposit 4–6 μm of CdTe at source and substrate temperatures of 610 °C and 510 °C respectively. The CdTe growth was performed in a two-stage process using: i) a 'higher pressure' growth at 30 Torr (3.99 kPa) in a nitrogen atmosphere (N₂) for 14 min and ii) a 'lower pressure' growth at 1 Torr (133.2 Pa) for 30 s. The growth at the higher pressure facilitates the growth of larger grains [11] while the growth at the lower pressure avoids the formation of pinholes. Specified sample were in-situ post CdTe growth annealed at 610 °C in the CSS chamber at an 'elevated' pressure of 200 Torr (26.66 kPa) for a specified time, details of which are outlined as they are discussed. Use of CSS deposition can lead to a non-uniform heating of the substrate, which in turn leads to varying thicknesses in the CdTe film resulting in variations in performance.

All samples were then treated with MgCl₂ at 430 °C for 20 min in an

air ambient unless stated otherwise [12]. Samples were etched with a nitric - phosphoric acid (NP) solution for 15 s following the chloride activation step in order to remove contaminants and to create a Te-rich surface. In specified samples a 5 nm layer of Cu was deposited via thermal evaporation at the back surface (dark side surface) to facilitate the formation of an Ohmic contact. All cells were completed by thermally evaporating 50 nm of gold to form the back contact. All cells had an active area of 0.25 cm².

Current density – voltage (JV) measurements were carried out under an AM1.5 spectrum at 1000 W m⁻² using a TS Space Systems solar simulator. External quantum efficiency (EQE) measurements were performed using a Bentham PVE 300 system. For focused ion beam (FIB) milling a FEI Helios Nano Lab 600 Dual Beam system, equipped with a focused 30 keV Ga liquid metal ion source was used. Imaging was carried out using a Hitachi Su70 SEM and electron beam induced current (EBIC) analysis using a Matelect ISM5 specimen current amplifier set to a 200 nA measurement range. The beam conditions used for EBIC analysis were 8 keV with a beam current of 0.92 nA. Secondary ion mass spectrometry (SIMS) was performed using Hidden Analytical gas ion and quadrupole detector. An O²⁻ ion gun was used to sputter the sample using a beam energy of 5 keV at a current of 300 nA, and the depth profiles were normalised. X - ray diffraction (XRD) spectra was carried out in a Rikaku® smart lab X-ray diffractometer at room temperature, using CuKα1 line as the X-ray source.

3. Results and discussion

3.1. Limitations of TCO/CdS/CdSe/CdTe device structure

Initially the impact of incorporating a CdSe layer into the conventional SnO₂/CdS/CdTe device structure (i.e. between the CdS and CdTe, see Fig. 1b) was investigated, with SnO₂ acting as the traditional HRT layer [7]. Both CdS and CdTe deposition conditions were kept the same as for our standard CdSe-free cell structure. It should be noted that for simplicity during initial process trials, Cu doping of the CdTe back surface was omitted [13–15]. This was done so as to isolate the influence of Se incorporation as much as possible, however this results in forward bias rollover for JV data and lower cell performance was expected [16]. Table 1 gives peak and average performance parameters extracted from JV data for cells with either a 0 nm, 50 nm or 100 nm thick CdSe layer. The JV and EQE curves for the highest efficiency contacts are shown in Fig. 2.

From this data it is clear that including the CdSe layer has a detrimental effect on performance, particularly by reducing J_{SC} from 18.7 mA cm⁻² to 15.6 mA cm⁻² and FF from 61.5% to 55.1% (for 100 nm of CdSe). The progressive reduction in FF is caused by an increase in series resistance (R_s) from 7.1 Ω cm⁻² to 8.6 Ω cm⁻² and

Table 1

Peak and average \pm standard deviation (SD) device parameters (in brackets) showing how the incorporation of CdSe into a FTO/SnO₂/CdS/CdTe device affects the working parameters, efficiency (η), short circuit current density (J_{SC}), open circuit voltage (V_{OC}) and fill factor (FF). CdS and CdTe thicknesses were 100 nm and 6 μ m, respectively. Cell were produced without a Cu layer or post growth annealing.

CdSe thickness (nm)	η (%)	J_{SC} (mA cm ⁻²)	V_{OC} (V)	FF (%)
0	9.9 (7.7 \pm 0.6)	18.7 (16.8 \pm 0.5)	0.78 (0.73 \pm 0.03)	68.2 (61.5 \pm 1.9)
50	8.0 (5.7 \pm 0.8)	15.0 (13.9 \pm 0.6)	0.76 (0.73 \pm 0.01)	65.3 (54.7 \pm 4.5)
100	7.1 (5.3 \pm 0.3)	15.6 (13.4 \pm 0.4)	0.76 (0.71 \pm 0.01)	59.7 (55.1 \pm 0.9)

12.6 Ω cm⁻² with the inclusion of 0 nm, 50 nm and 100 nm CdSe layers respectively. Shunt resistance (R_{SH}) values are unaffected by the CdSe incorporation. EQE curves show the origin of the J_{SC} losses: for devices that have 100 nm CdSe layers, the absorption was increased at long wavelengths, indicating the formation of a CdTe_(1-x)Se_x phase with a band gap of \approx 1.38 eV. However, there were significant losses at short wavelengths, with the absorption cut-off starting to occur at \approx 700 nm compared to \approx 550 nm for a device with CdS only. Inclusion of CdSe has increased the wavelength range over which harmful parasitic absorption takes place. In the ideal case the CdSe should completely convert to the photoactive CdTe_(1-x)Se_x zincblende phase, lowering CdTe band gap and inducing band gap grading to increase carrier lifetime [9]. There are therefore two possible explanations for the observed losses either, a) the CdSe layer is still present post CSS deposition and chlorine treatments, or b) in addition to intermixing with the CdTe, the CdSe also intermixes with the CdS layer forming a CdS_(1-x)Se_x phase. A mixed S-Se phase would be of a lower band gap than CdS and any absorption in this layer would be parasitic [2,17]. It is notable that for a 50 nm layer of CdSe the EQE data shows a very similar short wavelength cut-off to that of the 100 nm layer, but a lesser band gap shift at long wavelengths (\approx 1.41 eV). The inference here is that for the 50 nm layer there appears to be a lower Se content in the CdTe layer, but there is the same level of parasitic absorption to the 100 nm layer. If the observed losses were due to a residual CdSe layer we would anticipate this being far more pronounced for the 100 nm layer, hence this suggests the issue is the formation of a CdS_(1-x)Se_x phase. Paudel et al. [4] reported no such J_{SC} losses when CdS and CdSe were incorporated into the CdTe device structure possibly due to the differences in deposition conditions with ours favouring intermixing between the CdS and CdSe. Previous work has shown that the majority of the intermixing occurs during our CdTe deposition [5].

The nature of the short wavelength losses observed by EQE can be visualised via the use of EBIC analysis, with a high EBIC signal indicating regions of efficient carrier collection [18]. Fig. 3 shows overlaid secondary electron (red) and EBIC images (green) of device cross sections for CdS/CdTe and CdS/CdSe/CdTe. There are distinct differences in the collection for the two cells structures: The cell with no CdSe layer shows a more “typical” p-n junction response with high collection at CdS/CdTe interface and a poor collection towards the back surface of the cell [19].

In contrast the CdS/CdSe/CdTe cell shows little response at the CdS interface but collection throughout the remaining thickness of the cell. This is in accordance with EQE data presented in Fig. 2 and again suggestive of a photoinactive region, presumed to be CdS_(1-x)Se_x, being present at the near front surface. The presence of this unwanted interfacial layer has effectively buried the junction and is the cause of the reduced J_{SC} observed [20]. It is worth noting that the improved deep collection could be an indication of enhanced carrier lifetime via bandgap grading [8], but that the formation of CdS_(1-x)Se_x phases may be a fundamental limitation of incorporating a CdSe layer when using CdS and a high temperature CdTe deposition.

In order to determine whether the CdTe layer had completely converted to the CdTe_(1-x)Se_x phase XRD measurements of the CdTe back surface when deposited on CdSe and CdS are shown in Fig. S1. Swanson et al. [2] demonstrated a shift to higher angles in the XRD pattern for CdTe_(1-x)Se_x films compared to CdTe. From this data it is clear that no shift in the XRD pattern is observed as there is very little difference between the CdTe films with both exhibiting a highly (111) orientated zincblende CdTe film. This would indicate that the Se is not diffusing though the entirety of the CdTe film, forming a continuous CdTe_(1-x)Se_x phase. The CdTe thickness (5–6 μ m) and the interface being away from the back surface means we are unable to probe the Se content at the near interface using XRD.

3.2. Post CdTe growth annealing of CdS/CdSe/CdTe devices

The level of intermixing between CdTe and CdSe layers is liable to be controlled by two main factors, i) the CdTe deposition conditions and ii) the post-growth chloride treatment. The chloride treatment is widely associated with enhancing intermixing of the CdS and CdTe layers and improving the device performance [21]. However, it has been shown previously that for high temperature CSS-deposition the large CdTe grain structure, and subsequently the high activation energy required to recrystallize, is typically too high for intermixing to be significantly affected by the chlorine treatment. Instead the level of inter-diffusion is controlled primarily by the CdTe deposition conditions [5]. We observe a similar effect for Se diffusion, with there being little

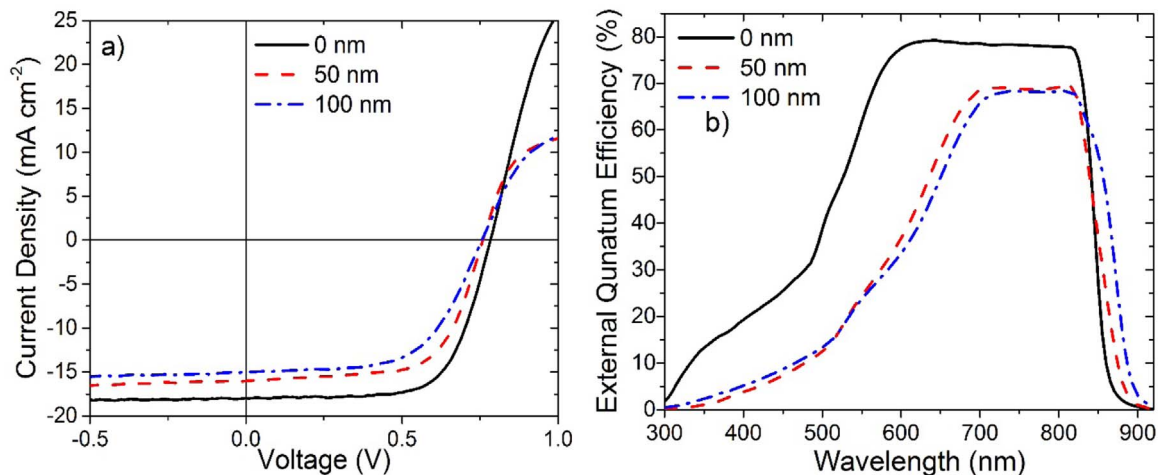


Fig. 2. a) JV and b) EQE responses as a function of CdSe thickness in CdS/CdSe/CdTe devices (for devices without Cu in the contacts or post growth annealing).

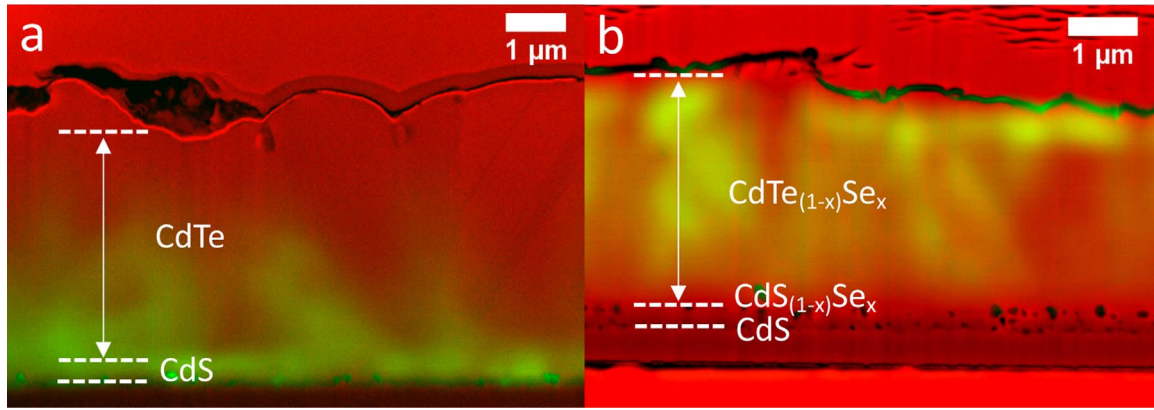


Fig. 3. Overlaid secondary electron (red) and EBIC output (green) for a) CdS/CdTe devices and b) CdS/CdSe/CdTe devices. The EBIC signal is overlaid on the SEM image to highlight the junction position. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

notable change in device performance when increasing the MgCl_2 annealing time from 20 min to 120 min (See Fig. S2).

Therefore, to enhance the amount of Se-Te inter-diffusion occurring during device fabrication, post growth annealing was performed in-situ in the CSS chamber at the growth temperature. Following completion of CdTe deposition the source temperature was maintained at 610 °C, but an elevated N_2 pressure of 200 Torr was used to suppress further sublimation. A series of cells were produced with such post growth annealing ranging from 0 min to 60 min Fig. 4 shows the JV and EQE responses for the highest efficiency contacts for the various annealing times, with peak and average performance parameters being given in Table 2. The post growth annealing shows some capacity to improve device performance, with all performance parameters being improved. J_{SC} is increased from 13.1 mA cm^{-2} to 18.3 mA cm^{-2} following a 60 min anneal, with peak performance occurring following a 20 min anneal; the EQE (Fig. 4b) shows that the annealing results in some enhanced collection at short wavelengths. This improvement in J_{SC} could be attributed to an increase in the availability of Se from the $\text{CdS}_{(1-x)}\text{Se}_x$ which has resulted in enhanced Se-Te intermixing. It is apparent from this EQE response, that while some additional Se-Te inter-diffusion has occurred during annealing, the performance is still limited. The collection at wavelengths close to the CdTe band-edge has also been enhanced which could indicate a wider depletion region resulting from increased carrier lifetimes. Alternatively, it could indicate that a better-quality junction has been formed via recrystallisation or improved inter-diffusion at the interface. It should also be noted that the $\text{CdTe}_{(1-x)}\text{Se}_x$ absorption cut-off doesn't change with increased

Table 2

Peak and average \pm SD device parameters (in brackets) for CdS/CdSe (100 nm) based cells as a function of in-situ post CdTe growth annealing times at 610 °C. Cells produced without a 5 nm Cu layer.

Annealing times (min)	η (%)	J_{SC} (mA cm^{-2})	V_{OC} (V)	FF (%)
0	7.1 (5.1 ± 0.3)	15.6 (13.1 ± 0.4)	0.76 (0.70 ± 0.01)	59.7 (55.2 ± 1.5)
20	9.7 (8.6 ± 0.2)	18.4 (16.8 ± 0.3)	0.77 (0.77 ± 0.01)	68.1 (67.0 ± 0.4)
40	9.2 (8.2 ± 0.3)	17.2 (17.6 ± 0.6)	0.78 (0.75 ± 0.01)	68.8 (62.1 ± 1.4)
60	9.0 (8.4 ± 0.1)	18.0 (18.3 ± 0.2)	0.75 (0.73 ± 0.01)	66.3 (62.9 ± 0.8)

annealing, which is suggestive of no significant change in the Se-Te intermixing. Whilst the average J_{SC} improves by annealing the devices for 60 min, the overall cell performance is reduced due to a reduced FF and V_{OC} .

3.3. Comparison of CdS and i-SnO₂ partner layers

Initial device testing strongly indicated that CdS was a limit to CdSe incorporation, potentially through the formation of a $\text{CdS}_{(1-x)}\text{Se}_x$ phases at the interface. To test this, the CdS layer was replaced as the n-type window layer with a 100 nm undoped SnO_2 layer and a 100 nm CdSe layer (see Fig. 1c) and cells were fabricated for comparison. SnO_2 was

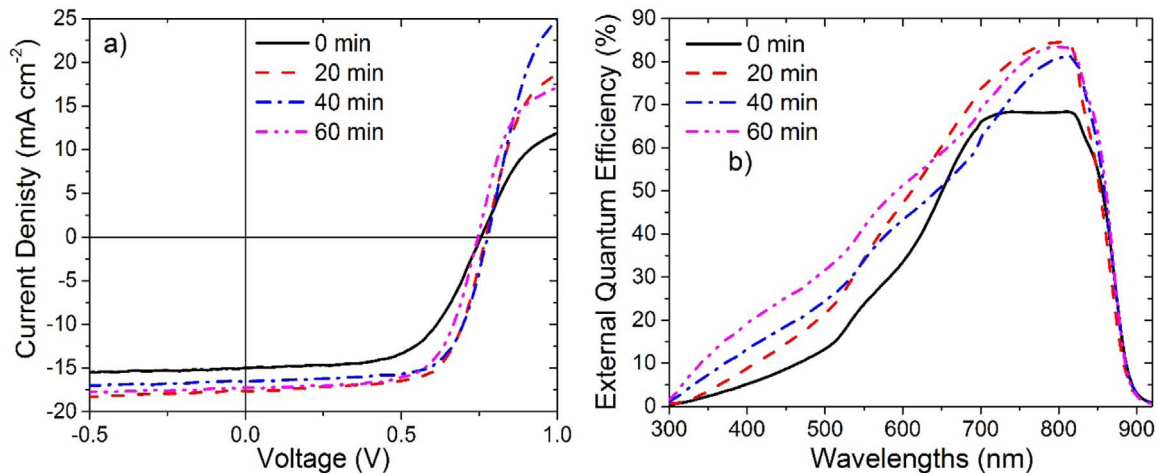


Fig. 4. a) JV and b) EQE data for highest efficiency contacts from cells produced using different in-situ post CdTe growth annealing times at 610 °C for CdS/CdSe (100 nm)/CdTe devices. Cells were produced without a Cu layer.

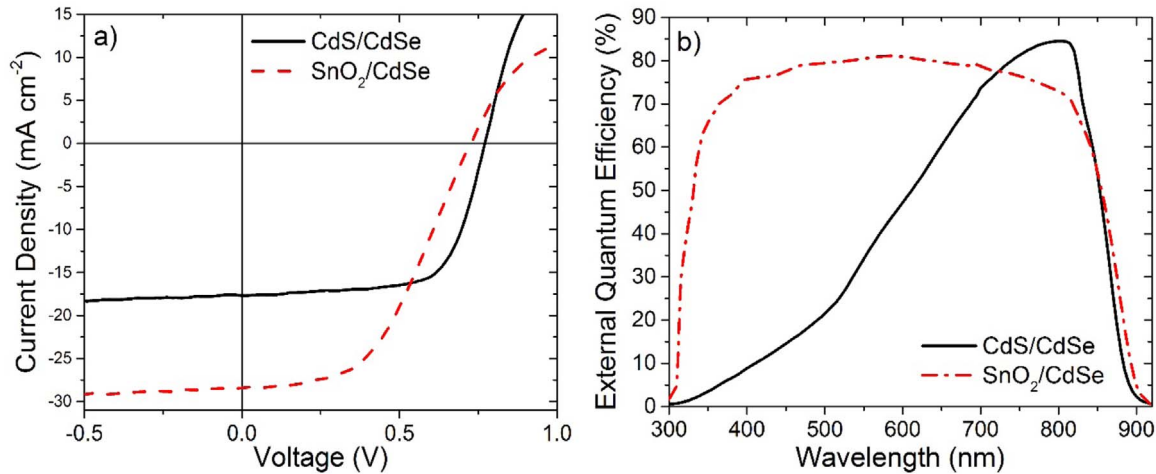


Fig. 5. a) JV and b) EQE data for cells produced using SnO_2 as the n-type window rather than the conventional CdS for CdSe (100 nm)/CdTe devices. Cells were produced with a 20 min in-situ post growth anneal at 610°C and no Cu was added to the back contact.

chosen due to its wide band gap (4 eV) and stability thus intermixing with CdSe should be negligible [22]. Previous work has shown that use of a CdSe layer without CdS leads to the gains in J_{SC} , but losses in both FF and V_{OC} [4]. It was hoped that by incorporating the SnO_2 layer such losses could be minimised. All CdTe growth conditions were kept identical, including the 20 min post deposition anneal at 610°C as this was shown to produce the best device response.

JV and EQE curves of the highest efficiency contacts for SnO_2/CdSe and comparative CdS/CdSe devices are shown in Fig. 5, with extracted average and peak performance parameters given in Table 3. SnO_2 based devices yielded a slightly higher peak efficiency due to a significant improvement in J_{SC} with peak value increasing from 18.4 mA cm^{-2} to 28.4 mA cm^{-2} . EQE analysis (Fig. 5b) of the SnO_2/CdSe device shows a near optimal shape, with minimal losses and significantly higher collection at short wavelengths. In addition to this the EQE response has been extended to longer wavelengths, indicating higher Se incorporation into the $\text{CdTe}_{(1-x)}\text{Se}_x$. From this result it is clear that the CdS is indeed the limiting factor, again presumably due to the formation of $\text{CdS}_{(1-x)}\text{Se}_x$ phases. The switch to a SnO_2 layer does however result in a drop in V_{OC} , with peak values decreasing from 0.77 V to 0.73 V. The device FF was also impacted falling from 68.1% to 48.5%, driven primarily by an increase in R_s which more than doubled from $6.6 \Omega \text{ cm}^{-2}$ to $13.5 \Omega \text{ cm}^{-2}$. This increase in R_s and drop in V_{OC} suggests that the $\text{SnO}_2/\text{CdTe}_{(1-x)}\text{Se}_x$ interface is not of as high quality as the CdS/CdTe or CdS/CdTe $_{(1-x)}\text{Se}_x$ interfaces [2]. Following the switch from a CdS to SnO_2 layer a degree of process re-optimisation was required. Device annealing post-CdTe deposition had the most impact on CdS/CdSe devices, hence this process was re-assessed for SnO_2/CdSe based cells. Devices were annealed following CdTe deposition in the CSS chamber at 610°C for either 0 min, 20 min or 40 min, with the influence on performance being shown in Fig. 6. Associated JV and EQE curves for highest efficiency contacts are shown in Fig. 7a and b respectively. Additionally, due to the high degree of back contact related rollover

observed for these devices (see Fig. 5a), 5 nm of Cu was included into the device back surface to minimise rollover and improve the FF [13]. Initial sample sets had not included Cu so the effect of Se could be investigated without being influenced by Cu. However it was expected the optimal $\text{SnO}_2/\text{CdSe}/\text{CdTe}$ would require Cu inclusion, hence all devices discussed from this point include Cu in the device structure.

Devices with no post growth annealing (0 min) have low performance, with an average efficiency of only 5.5%. Annealing the devices for 20 min significantly improves the performance, with all device parameters improving and giving an average performance of 11.3%. EQE analysis (Fig. 7b) shows an improvement at short wavelengths, indicating this post-growth annealing is influencing the near interface region, and results in a J_{SC} improvement from 21.6 mA cm^{-2} to 29.6 mA cm^{-2} . Annealing the devices for longer leads to a loss in performance with the average dropping to 9.7%, with J_{SC} and FF dropping but V_{OC} being maintained. The drop in FF is due to R_s increasing from $5.6 \Omega \text{ cm}^{-2}$ to $7.9 \Omega \text{ cm}^{-2}$ and R_{SH} decreasing from $727.7 \Omega \text{ cm}^{-2}$ to $538.7 \Omega \text{ cm}^{-2}$, this suggests that the devices have now become over treated and results in a lower performance. A range of CdSe thicknesses of 50 – 400 nm were similarly evaluated with 100 nm being found to give the highest device performance (see Supplementary Fig. S3). CdSe layers > 100 nm thick resulted in significant J_{SC} losses via parasitic absorption. For thicker films this could be corrected partially by additional annealing (this is shown for a 200 nm film in Fig. S4 and Table S1) but performance remained significantly lower than for 100 nm CdSe. Under these conditions it would appear there is a limit to the CdSe that can effectively be incorporated.

Poplawsky et al. [8] suggested that the CdSe wurzite phase is photoinactive whereas the $\text{CdTe}_{(1-x)}\text{Se}_x$ zincblende structure is photoactive. We may postulate then that the unannealed samples retain some of the unconverted CdSe phase, resulting in a lower performance. Annealing has the effect of fully converting remaining CdSe to the $\text{CdTe}_{(1-x)}\text{Se}_x$ phase. The general improvement in device performance parameters would also suggest this, as the resistive losses have decreased and the V_{OC} has increased, indicating a more favourable interface and reduced recombination. The lower V_{OC} for CdSe/CdTe based devices compared to CdS/CdTe, could be due simply to the $\text{CdTe}_{(1-x)}\text{Se}_x$ phase being of a lower band gap compared to CdTe, $\approx 1.38 \text{ eV}$. For the case of an effectively graded bandgap and thus increased carrier lifetime we may anticipate an improved V_{OC} . However if the bandgap of the CdTe layer has simply been uniformly reduced the maximum achievable V_{OC} for $\text{CdTe}_{(1-x)}\text{Se}_x$ will likewise be lowered [23].

SIMS was used to investigate the Se distribution in each sample as a function of annealing time, Fig. 8 shows normalised Se spectra for the three devices. The addition of the annealing stage has induced some

Table 3

Peak and average \pm SD of device performance (in brackets) parameters for cells using CdS or SnO_2 as the device window layer in CdSe (100 nm)/CdTe devices. Cells were produced with a 20 min in-situ post growth anneal at 610°C and no Cu was added to the back contact.

Window layer	η (%)	J_{SC} (mA cm^{-2})	V_{OC} (V)	FF (%)
CdS/CdSe	9.7	18.4	0.77	68.1
	(8.6 ± 0.2)	(16.8 ± 0.3)	(0.77 ± 0.01)	(67.0 ± 0.4)
SnO_2/CdSe	10.1	28.4	0.73	48.5
	(6.2 ± 0.9)	(21.7 ± 1.4)	(0.65 ± 0.03)	(42.7 ± 2.6)

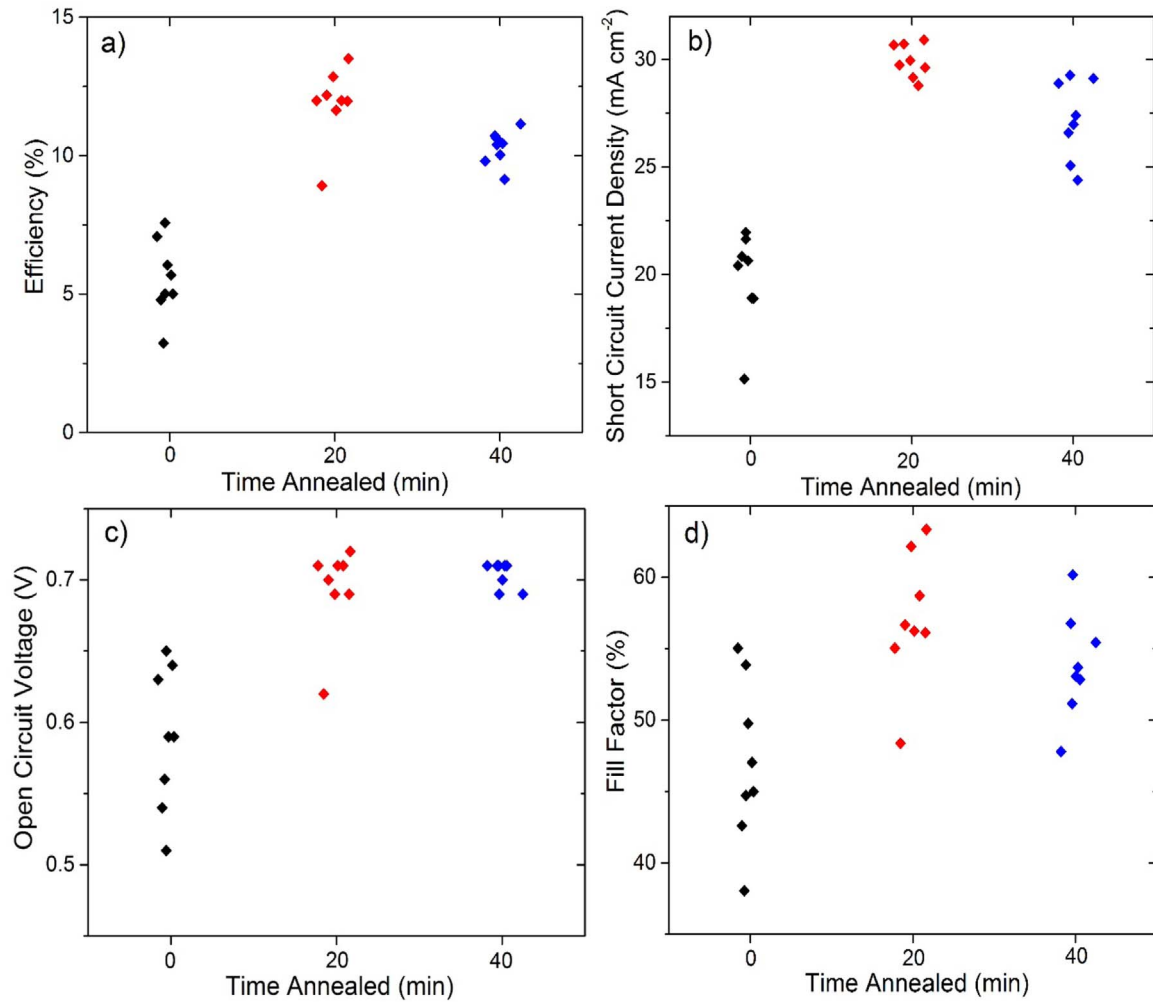


Fig. 6. SnO₂/CdSe (100 nm)/CdTe device performance parameters a) efficiency, b) J_{SC} , c) V_{OC} and d) FF for cells produced using different in-situ post CdTe growth annealing times at 610 °C. A 5 nm layer of Cu was added to the back contact.

additional Se diffusion into the CdTe layer, with the 20 min and 40 min anneals showing higher Se content throughout the CdTe layer. The 40 min sample also shows a more uniform distribution than the 20 min anneal, however there is little suggestion of Se grading. In the ideal scenario the Se will be graded with higher content at the near interface, thus a lower bandgap, with decreasing Se content towards the back

surface. Instead we see high Se content at the near interface then a reasonably linear content in the bulk. Sharp increases observed at the back surface are an artefact of the measurement, due to a change in the ion yield in the pre-equilibrium region during the early stage of the sputtering process. From the data presented it is evident that post-growth annealing may alter the Se content in the CdTe/CdTe_(1-x)Se_x

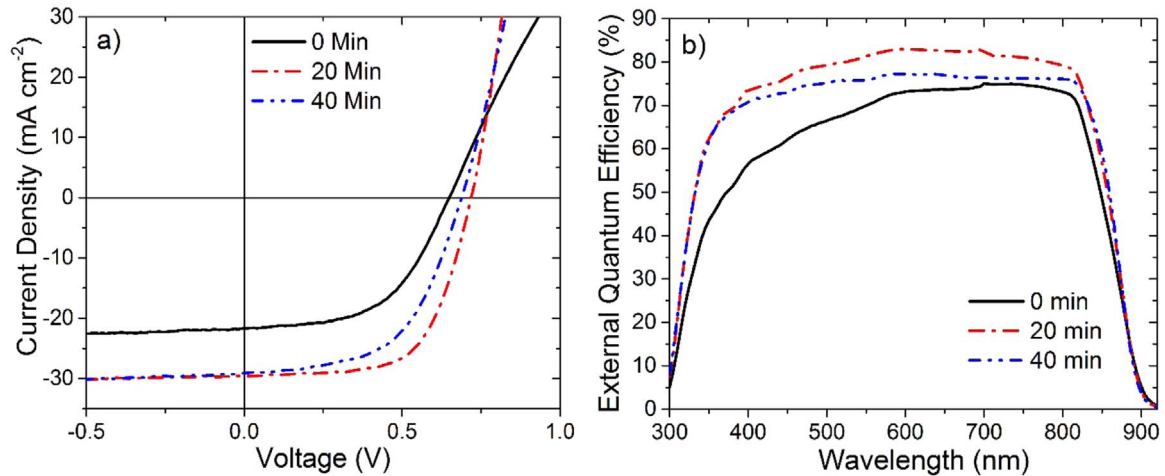


Fig. 7. a) JV and b) EQE data for highest efficiency contacts from cells produced using different post CdTe growth in-situ annealing times at 610 °C on SnO₂/CdSe (100 nm)/CdTe based devices. A 5 nm layer of Cu was added at the back contact.

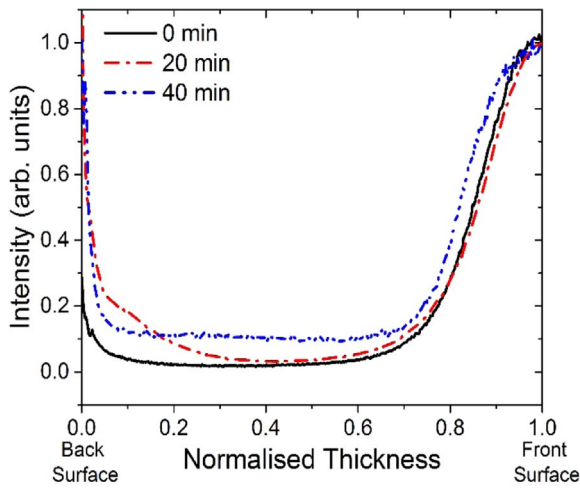


Fig. 8. Secondary ion mass spectrometry (SIMS) data showing the Se distribution through the sample as a function of annealing time with 1 representing the front SnO_2 interface and 0 representing the back surface. Counts have been normalised to 1 with respect to the Se content at the SnO_2 interface to allow direct comparison between the profiles.

Table 4

Peak and average \pm SD device parameters (in brackets) when using ultrathin CdS, FTO, ZnO and TiO_2 as the n-type window layer. The SnO_2 based devices are also shown for comparison. Cells were in-situ post growth annealed at 610°C for 20 min and a 5 nm Cu layer was added at the back contact.

Device structure	η (%)	J_{SC} (mA cm^{-2})	V_{OC} (V)	FF (%)
SnO_2/CdSe	13.5 (11.3 \pm 0.8)	29.6 (29.5 \pm 0.8)	0.72 (0.69 \pm 0.01)	63.3 (54.9 \pm 2.6)
$\text{SnO}_2/\text{CdS}/\text{CdSe}$	11.8 (11.1 \pm 0.2)	23.6 (24.1 \pm 0.3)	0.73 (0.73 \pm 0.01)	68.2 (63.6 \pm 1.3)
FTO/ CdSe	11.3 (9.5 \pm 0.8)	29.8 (28.6 \pm 0.4)	0.66 (0.63 \pm 0.02)	57.5 (52.3 \pm 2.4)
ZnO/ CdSe	9.5 (8.6 \pm 0.6)	28.8 (27.4 \pm 0.5)	0.66 (0.62 \pm 0.01)	50.2 (50.1 \pm 1.2)
TiO_2/CdSe	6.1 (5.5 \pm 0.2)	27.5 (25.8 \pm 0.4)	0.74 (0.71 \pm 0.02)	30.0 (30.5 \pm 1.6)

however in order to achieve an ideally graded band gap some greater refinement in control of the Se diffusion may be required.

3.4. Alternatives to SnO_2 as the device window layer

In order to try and improve the V_{OC} and FF produced by $\text{CdTe}_{(1-x)}\text{Se}_x$

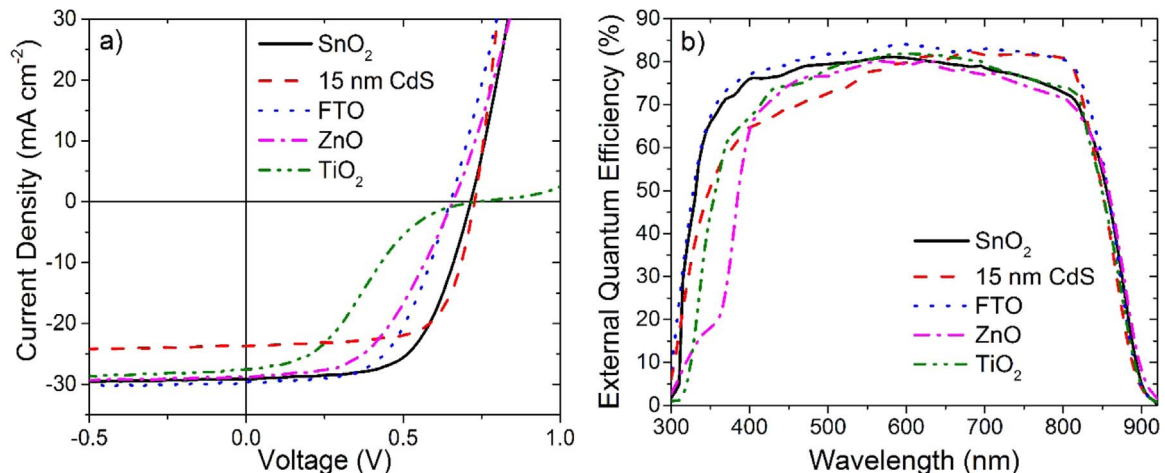


Fig. 9. a) JV and b) EQE response comparison for cells using ultrathin CdS, FTO, ZnO and TiO_2 as the window layer in CdSe/CdTe photovoltaics. Cell were in-situ post growth annealed at 610°C for 20 min and a 5 nm Cu layer was added at the back contact.

Table 5

Peak and average \pm SD device parameters (in brackets) for cells using SnO_2/CdSe (100 nm) and CdS (100 nm) with a 5 nm Cu layer at the back contact and a 20 min in-situ post growth anneal at 610°C .

Window layer	η (%)	J_{SC} (mA cm^{-2})	V_{OC} (V)	FF (%)
SnO_2/CdSe	13.5 (11.3 \pm 0.8)	29.6 (29.5 \pm 0.8)	0.72 (0.69 \pm 0.01)	63.3 (54.9 \pm 2.6)
SnO_2/CdS	14.0 (13.1 \pm 0.2)	25.6 (24.4 \pm 0.4)	0.82 (0.81 \pm 0.01)	66.4 (66.5 \pm 0.9)

based devices different window layers were investigated as alternatives to SnO_2 . The layers compared were FTO (i.e. no additional layer), 100 nm ZnO, 50 nm TiO_2 and ultrathin (15 nm) CdS; all devices were processed identically utilising the optimal conditions shown in Section 3.3. Table 4 shows the influence of the different layers on the peak and average device parameters along with SnO_2 based devices shown for comparison. Fig. 9a and b show the JV and EQE responses produced by the highest efficiency contacts from each device.

Of the window layers compared in this study, SnO_2 based devices showed both the highest peak and average performance. Devices with an ultrathin CdS layer showed a similar average performance to SnO_2 , although peak efficiency is slightly lower. Other partner layers typically show significantly reduced performance. The CdS based devices show an enhanced average FF compared to the SnO_2 devices, 63.6% and 54.9% respectively, and improved average V_{OC} from 0.69 V to 0.73 V, however peak V_{OC} values are similar. The improvement in FF and V_{OC} would seem to confirm that the $\text{CdS}/\text{CdTe}_{(1-x)}\text{Se}_x$ interface is of a better quality than the $\text{SnO}_2/\text{CdTe}_{(1-x)}\text{Se}_x$ interface. However, the overall performance is reduced due to a significant reduction in device J_{SC} , via the formation of a $\text{CdS}_{(1-x)}\text{Se}_x$ layer, visible in EQE losses < 600 nm, even at this significantly reduced CdS thicknesses.

The devices which utilise FTO and ZnO as device window layers show a further reduction in performance due to a significant decrease in V_{OC} with the peak dropping from 0.72 V for the SnO_2 cells to 0.66 V for both the FTO and ZnO devices respectively. This indicates that these layers are unsuited to $\text{CdTe}_{(1-x)}\text{Se}_x$ devices, either due to a poor quality junction or low built in voltage, despite the high current that can be achieved.

TiO_2 based devices show a particularly pronounced reduction in efficiency (to an average of 5.5%) due to a low FF with an average of 30.3%. This results from the formation of an uncharacteristic S-shaped curve in the JV data at forward bias [24]. The S-shaped “kink” is not widely observed for CdTe devices but is identified as an interfacial barrier due to a misalignment of the energy bands through either an

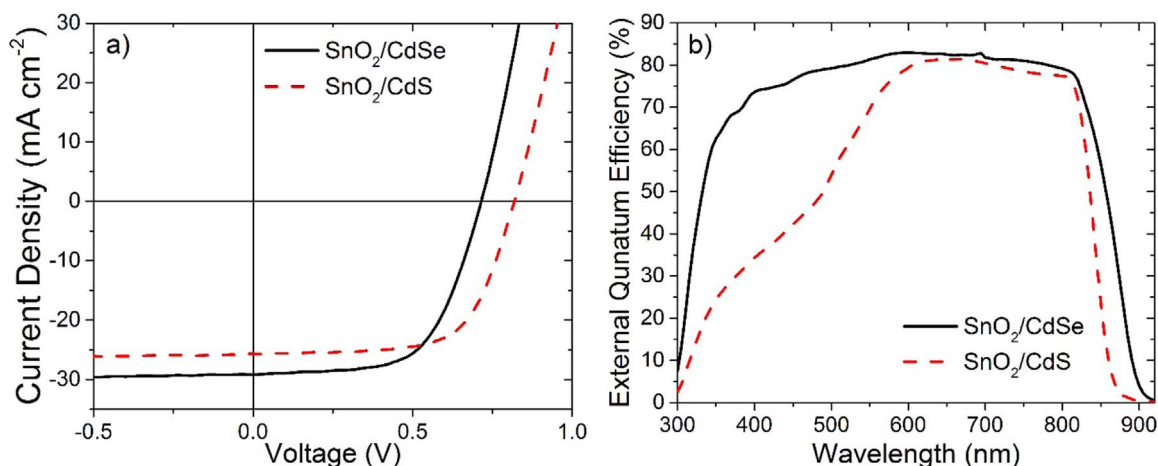


Fig. 10. a) JV and b) EQE data for highest efficiency contacts from cells using SnO₂/CdSe (100 nm) or SnO₂/CdS (100 nm) as the device window layers with a 5 nm Cu layer at the back contact and a 20 min in-situ post growth anneal at 610 °C.

extraction or injection barrier in organic PV [22,25].

These comparative results demonstrate the importance of the correct choice of partner layer for CdSe based devices. Whilst high J_{SC} values are obtainable with a variety of partner layers, the losses experienced in V_{OC} and FF are controlled by the partner layer. From the development work the most suitable window structure was identified to be SnO₂ coupled to 100 nm of CdSe, with a post-growth anneal of 20 min at the growth temperature (610 °C) in-situ. Here we directly compare the performance of our FTO/SnO₂/CdSe structure with a standard FTO/SnO₂/CdS (100 nm) structure. Table 5 gives peak and average performance parameters with JV and EQE curves for the highest efficiency contacts shown in Fig. 10a and b. The peak performance of both devices is similar being 13.5% for the CdSe device and 14.0% for the CdS. The CdSe based device shows a very high J_{SC} of 29.6 mA cm⁻² (with primary losses associated with reflection from the glass substrate and TCO) compared to 25.6 mA cm⁻² when CdS is used.

The devices with CdSe have a significantly lower V_{OC} of 0.72 V compared to 0.82 V for CdS based devices, whilst the CdS based devices also have a marginally higher FF. The loss in V_{OC} could be due to a number of reasons: a) for the CdSe based device the band gap of the absorber layer CdTe_(1-x)Se_x has been lowered (≈ 1.38 eV from EQE estimation) which in turn means the maximum attainable V_{OC} has been reduced. It should be noted that both CdSe and CdS structures show a similar voltage deficiency relative to their band gap, 52.8% and 54.6% respectively or; b) the SnO₂/CdTe_(1-x)Se_x interface is of a lower quality leading to high interfacial recombination and thus a reduced V_{OC} .

4. Conclusion

Through the cell led work in this paper we have identified a number of key factors related to the incorporation of CdSe layers into CdTe solar cell structures. We established that the CdS/CdSe/CdTe device structure may be fundamentally limiting due to enhanced optical losses. It is suggested that this results from the diffusion of the Se into the CdS layer, leading to the potential formation of parasitic CdS_(1-x)Se_x phases and hence the observed reduction in device J_{SC} . Device current can be significantly increased by removing the CdS layer from the device structure and replacing it with a SnO₂ layer. It was found that in-situ post CdTe growth annealing was essential to achieve a high current, as it appears to modify Se diffusion into the CdTe layer i.e. it aids conversion from residual CdSe to the reportedly photoactive CdTe_(1-x)Se_x (zincblende) structure. Since such post growth annealing was shown to result in an improved device performance, it is necessary to further investigate the role of the post growth process to achieve finer control, as no evidence of effective Se-grading throughout the CdTe layer was

observed. This served to demonstrate though that CdSe/CdTe devices require different processing approaches to those for the established CdS/CdTe device structure.

Following optimisation a SnO₂/CdSe/CdTe cell of up 13.5% was achieved, compared to 14.0% for an equivalent SnO₂/CdS/CdTe devices. J_{SC} values were significantly higher for the CdSe based cell but losses occurred due to a lower V_{OC} . However, there remains significant scope for improvement in CdSe based devices which may allow for the V_{OC} to be increased. Initial investigations demonstrated that replacing the SnO₂ with other alternatives such as TiO₂, ZnO and FTO led to a further reduction in the V_{OC} , highlighting that the choice of appropriate window layer partner is essential and improving this partner layer is the route to overcoming the V_{OC} deficit. Such improvement may involve varying the conditions of the SnO₂ deposition e.g. deposition temperature, surface treatments etc, or investigating alternative oxides (e.g. Mg_xZn_(1-x)O [7,26]).

Overall this work demonstrates the feasibility of oxide/CdSe structures as a window for CdTe but that significant further work is required to establish: i) how Se diffusion can be better controlled and whether grading can be achieved; ii) whether interfacial recombination is a dominant issue with oxide partner layers; and iii) the optimal band alignment for the oxide partner layer and use this to identify feasible alternatives to CdS.

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Data availability

The data which supports the findings of this work is available from Liverpool's Data Catalogue or from the author.

Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at <http://dx.doi.org/10.1016/j.solmat.2018.03.010>.

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